Code No: P21ECT02

HALL TICKET NUMBER

PACE INSTITUTE OF TECHNOLOGY & SCIENCES::ONGOLE
(AUTONOMOUS)
II B.TECH ISEMESTER END REGULAR EXAMINATIONS, JAN - 2023
SWITCHING THEORY AND LOGIC DESIGN
(ECE Branch)

Time: 3 hours Max. Marks: 70

Answer all the questions from each UNIT (5X14=70M)

Q.No.		Questions	Marks	C	KL
		UNIT-I			
1.	a)	Encode the decimal numbers using 6, 3, 1,-1 weighted code. Is it a self-complementing code?	[7M]	1	2
	b)	Generate Hamming code for a 4-bit Excess-3 message to detect and correct single-bit errors.	[7M]	1	3
		OR			
2.	a)	Reduce the following function using the k-map technique. F(A,B,C,D)=∏M(1,2,3,5,6,7,8,9,12,13)	[7M]	1	2
	b)	Simplify the Boolean function F using the don't care conditions d, in (i) sum of products and (ii) product of sums. F= A'B'D' + A'CD+A'BC	[7M]	1	3
		UNIT-II			
3.	a)	Implement the following function using only NAND gates G=(a + b).(c. d + e)	[7M]	2	3
	b)	Perform the realization of full subtractor and full adder using decoders and logic gates.	[7M]	2	2
		OR			
4.	a)	Explain the realization using Multilevel NAND-NOR gates	[7M]	2	2
	b)	Explain the operations of the Carry look-ahead adder.	[7M]	2	3
		UNIT-III			
5.	a)	Design a 4-bit binary comparator with basic gates.	[7M]	3	3
	b)	Write a brief note on the Architecture of PLDs	[7M]	3	2
		OR			
6.	a)	Realize the function f(A,B,C,D) = Σ(1,2,5,6,7,8,10,14,15) using i) 8:1 MUX ii) 4:1 MUX	[7M]	3	3
	b)	Implement f (A, B, C, D) = Σ(0,1,3,5,6,8,9,11,12,13) using PAL and explain its procedure.	[7M]	3	3
		UNIT-IV			
7.	a)	What is race around the condition and how to avoid it along with the circuit diagram?	[7M]	4	2
	b)	Design a mod-12 Ripple counter using T flip flops and explain its operation.	[7M]	4	3
		OR			

8.	a)	Realize D-latch using R-S latch. How it is different from D-flip flop. Draw the circuit using NAND gates and explain.	[7M]	4	3
	b)	Convert JK flip-flop to T flip-flop.	[7M]	4	2
		UNIT-V			
9.	a)	Find the equivalence partition and a corresponding reduced machine in a standard form for a given machine.	[7M]	5	3
	b)	Explain the procedure of Meelay to Moore conversion.	[7M]	5	2
		OR			
10.	a)	The output Z of a fundamental mode, two input sequential circuit is to change from 0 to 1 only when x2 changes from 0 to 1 while x1=1. The output changes from 1 to 0 only when x1 changes from 1 to 0 while x2=1. Find a minimum row reduced flow table.	[7M]	5	3
	b)	Draw the diagram of Mealy-type FSM for the serial adder.	[7M]	5	2

PS	NS , Z	
	X=0	X=1
A	C,1	E,1
B	A,0	D,1
C	E,0	D,1
D	F,1	A,1
E	B,1	F,0
F	B,1	C,1

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